TWO’S COMPLEMENT FAST SERIAL - PARALLEL MULTIPLIERS BASED ON ZERO - MSB - OF - MULTIPLIER SCHEME

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Abstract- In this letter, two fast serial-parallel multipliers based on Zero – MSB - OF –Multiplier (ZMM) scheme are proposed. The proposed multipliers consisting of a single row of logic gates necessitate zero MSB of the multiplier.

Indexing terms: – Digital arithmetic, multiplying circuit

I. INTRODUCTION

The bit-serial multipliers are used in digital signal processing for implementation of discrete orthogonal transforms, convolutions and in digital filtering applications. For multiplication of signed bits in two’s complement from several multipliers are proposed. Moh and Yoon [1] proposed a serial-parallel multiplier for two’s complement number based on sign-bit extension. But the multiplier requires additional gate delay. Lu and Kenney [2] presented a two’s complement most significant-bit-first add and shift serial multiplier. The design consisting of three major components is very much complicated and requires more hardware. Sunderet at [3] have presented a two’s complement multiplier based on Baugh-Wooley algorithm which is faster, needs less hardware and has lower area-and time-complexities but the output bits are not obtained a sequence. The multiplier proposed by Nayak and Meher [4] is still simpler and efficient, but requires more hardware.

In general, the multipliers for sign-bit numbers are complicated and require more hardware compared to multipliers using unsigned bit. So, in this paper we propose Zero-MSB-of-Multiplier (ZMM) scheme of multiplication of sign-bit numbers to achieve considerable simplicity in architecture in addition to less hardware requirement and high throughput. Two simple serial-parallel multipliers based on ZMM scheme are presented. In this scheme, the MSB of the multiplier should be ‘0’. If the MSB of the multiplier is ‘1’, the number is converted into two’s complement from before feeding serially into the multiplier. Again, if the MSB of the multiplier is ‘0’, the product is obtained directly. However if the MSB of the multiplier is ‘1’, the output from the multiplier is reconverted into two’s complement form to get the real product.

II. MATHEMATICAL BACKGROUND

By multiplying arbitrary n-bit two’s complement numbers A and B, the product P can be expressed by

\[ P = A \cdot B = \left( -2^{n-1} a_{n-1} + \sum_{j=0}^{n-2} 2^j a_j \right) \left( -2^{n-1} b_{n-1} + \sum_{j=0}^{n-2} 2^j b_j \right) \] ………………… (1)

Since \( b_{n-1} = 0 \) in ZMM scheme.
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\[ P = -2^{n-1} a_{n-1} \sum_{j=0}^{n-2} 2^j b_j + \sum_{j=0}^{n-2} 2^{i+j} a_i b_j \]  
(2)

\[ P = 2^n \sum_{j=0}^{n-2} 2^j (a_{n-1} b_j - 1) + \sum_{j=0}^{n-2} 2^{i+j} a_i b_j \]  
(3)

\[ P = \sum_{i=0}^{n-2} \sum_{j=0}^{n-2} 2^{i+j} a_i b_j + 2^{n-1} \sum_{j=0}^{n-2} 2^i a_{n-1} b_j - 2^{2n-1} + 2^{2n-2} + 2^{n+1} \]  
(4)

Equation 2 may also be expressed as

\[ P = -2^n \sum_{j=0}^{n-2} 2^j a_{n-1} b_j + 2^{n-1} \sum_{j=0}^{n-2} 2^i a_{n-1} b_j + \sum_{i=0}^{n-2} \sum_{j=0}^{n-2} 2^{i+j} a_i b_j \]  
(5)

Equations 4 and 5 can be easily applied to serial parallel multipliers.

Implementation of two’s complement bit level multiplication:

**Multiplier-I**

Equation 4 is implemented in the proposed multiplier-1, shown in fig.3. An example of 4×4 two’s complement multiplication of numbers 3 and -5 is shown in fig.1. First the multiplier -5 is converted into +5 according to ZMM scheme and the product of 3 and 5 is implemented in the multiplier.

The proposed multiplier-I consists of four units- two conversion units, a logic unit and an adder unit. Each conversion unit at the input and output consists of a XOR gate and a full adder. Both conversion units are controlled by the signal Q which is ‘00000000’ if MSB of the multiplier is ‘0’ AND ‘11111111’ if MSB is ‘1’. The multiplier bits and the control signal Q are fed simultaneously to the XOR gate of input conversion unit. However, the same control signal Q is fed to the XOR gate of the output conversion unit staggered by 3 time steps. Another control signal Q’ is fed to the full adders of both conversion units. Q’ is 00000000 if the MSB of the multiplier is ‘0’ and 00000001 if MSB is ‘1’. However, Q’ is fed to the full adder of the output –conversion unit staggered by 3 time steps. So that if the multiplier is a positive number, it is available as such at the logic gates and the final product is available directly at the output. If the multiplier is a negative number, its two’s complement form is available at the output.
logic gates and the final product is available at the output after two's complement conversion of multiplier output. The logic unit consists of (n-1) AND gates and one NAND gate. Each bit from conversion unit is available to all the logic gates simultaneously. The bits of the multiplicand are stored at the individual gates. The duration of the clock cycle is $T_A'$ which is the full adder delay, since the gate delay is comparatively smaller. The extra '1' for the fourth column is provided to the right most adder of the adder unit with the help of Q11 signal. Four MS bits are appended to the left of MSB of the multiplier for input! output synchronization. As four zeros are appended to the left of the MSB of the multiplier, the '1' in the eighth column is obtained by NANDing the fourth bit of the fifth partial product. Since final product could be a 2n –bit two’s complement number, all excessive carry-outs after eight bit should be ignored. The output of the multiplier is then converted into two’s complement form as 11110001(-15), which is the product of 3 and -5.

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### Multiplier -II

Eqn. 5 is implemented in the proposed multiplier - II, shown in Fig. 4. The first term of eqn.5 necessitates sign- bit extension. For multiplication 3 and -5, the multiplier -5 is converted into +5 according to ZMM scheme. The multiplication of 3 and 5 based on sign-bit extension is shown in Fig.2. The sign-bit extension is effected either as a direct extension of partial product or created as a result of carry generated by the addition of previous row. The output of the multiplier is converted into its two's complement form as 11110001 (-15) which is product of 3 and -5. The proposed multiplier-II has same four units as multiplier-I. The conversion units function in the same manner with the help of same control signals Q and Q1 as in multiplier-I. However both signals are fed to the XOR gate of the output conversion unit and output adder, respectively, staggered by 2 time-steps. The logic unit consists of n AND gates. The OR gate in the left most adder of the adder unit provides necessary sign-bit extension.

### III.CONCLUSION

The VLSI performance measures of multipliers of [1], [2] and proposed multipliers-I and II are respectively, 11.93 x $10^6$, 3.01 x $10^6$, 1.10 x $10^6$ and 0.98 x $10^6$.

### IV. REFERENCE

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