CMOS Based Design Simulation Of Adder /Subtractor Using Different Foundries

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Abstract: In this paper a 4 bit parallel adder/subtractor circuit has been designed and analyzed. The circuit uses a controlled adder/subtractor circuit which converts the negative numbers into their 2’s complement. A comparative study of the silicon area and the power consumption has been done in the circuit using different channel lengths such as 65nm, 45nm. The circuit is designed and simulated using DSCH schematic tool and the layout is developed by Microwind VLSI CAD Tool. The designed circuit has shown a remarkable reduction in the consumed power of 93% and a reduction of 49% in consumed area in 45nm foundry as compared to 65nm foundry. The simulation has been done using BSIM4 device modeling.

Keywords - Full Adders, Full Subtractors, Controlled Inverters, CMOS.

1. INTRODUCTION

Addition forms the basis for many processing operations, from counting to multiplication to filtering. As a result, adder circuits are of great interest to digital system designers. Adders and Subtractors are important components in the applications like Digital Signal Processing (DSP)architectures. For signal processing, digital full-adder and full-subtractor are the basic logic circuits which can find applications in digital computing and packet labels processing [1]. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor [2]. The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems [3]. Computations need to be performed using low-power, area-efficient circuits operating at greater speed [2].

The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices [2]. The power consumption in a CMOS digital circuit can be calculated using Eq.1. Whether it is a general-purpose system or an application specific processor, addition is by far the most frequently used operation.

\[
P = fCV_{dd}^2 + f' I_{off}V_{dd} + I_{off}V_{dd}
\]

(1)

Full Adders - A full Adder is a combinational circuit that performs addition of two bits taking into consideration about a 1 that may have generated by the previous stage as shown in Figure (1). The circuit
The circuit has 3 inputs A, B, Cin and two outputs S and Cout. The inputs A and sum B are the bits to be added and Cin is the carry from the previous stage while S is the output sum and Cout is the output carry as in Eq. 2 and Eq. 3.

\[
\text{Sum} = A \oplus B \oplus \text{Cin} \tag{2}
\]

\[
\text{Cout} = (A \cdot B) + (\text{Cin} \cdot (A \oplus B)) \tag{3}
\]

**Full Subtractors** - A full subtractor is a combinational circuit that performs a subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage[3] shown in figure(2).

The circuit has 3 inputs A, B, BOR_{IN} and two outputs D and BOR_{OUT}. The inputs A, B, BOR_{IN} are the minuend, subtrahend and previous stage borrow respectively while D is the output Difference and BOR_{OUT} is the output Borrow as in Eq.4 and Eq. 5.

\[
\text{BOR}_{OUT} = \text{BOR}_{IN} (A' B' + AB) + A' B \tag{4}
\]

\[
\text{Difference} = A \oplus B \oplus \text{BOR}_{IN} \tag{5}
\]

In this paper a unified adder/subtractor circuit has been analyzed which performs the addition as well as subtraction of two 4 bit binary numbers. The circuit also detects the overflow if occurs in case the sum exceeds the permissible limit of the circuit.

**II. ADDER/ SUBTRACTOR CIRCUIT**

In this paper a 4 bit unified parallel adder/subtractor circuit with a overflow detector is analyzed. Subtraction of two binary numbers can be accomplished by adding 2’s complement of the subtrahend to the minuend [5] shown in figure(3).
The circuit uses 4 units of full adders and a separate XOR gate is used to detect any overflow in the circuit. This circuit performs both the operations of addition as well a subtraction. The bits of the binary number $B_3B_2B_1B_0$ are fed to the controlled inverter which is a XOR gate. The 4 bit binary number $A_3A_2A_1A_0$ is added to a 4 bit binary number $B_3B_2B_1B_0$ when the mode control bit $M$ is in logic 0 state. When the input $M$ is in logic state 1 then the binary number $B_3B_2B_1B_0$ in the present state gets complemented. If the same 1 is also fed in the carry in of the LSB Full adder then the 2’s complement of binary number $B_3B_2B_1B_0$ is added to the binary number $A_3A_2A_1A_0$. The output of the circuit in this case is the subtraction of the two numbers that is $A-B$. This circuit also indicates the occurrence of the Overflow if the output exceeds the permissible limit of the circuit. The carry out $C_3$ from third full adder stage and the carry out $C_4$ from fourth full adder stage is given as input in the XOR gate to give the overflow. The output OVERFLOW of the circuit gives a logic 1 if overflow occurs, else it remains in the 0 state.

III. SCHEMATIC DESIGN SIMULATION

The schematic design of the 4 bit composite parallel adder-subtractor is shown in figure (4) and is drawn in DSCH tool and its working is verified in accordance to its truth table. If the control input $M$ is low then the circuit behaves as an Adder and when it is High the circuit behaves as a Subtractor. The subtraction operation is converted into addition by complementing the minuend by passing it through the XOR. If a result of an n-bit addition does not fall within the allowed range, then an arithmetic overflow occurs.[6]. The controlled input $M$ modifies the behavior of circuit according to Table 1.

Table 1: Behaviour of Circuit

<table>
<thead>
<tr>
<th>M</th>
<th>Behaviour of circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Adder</td>
</tr>
<tr>
<td>1</td>
<td>Subtractor</td>
</tr>
</tbody>
</table>
The circuit behaviour for input conditions

a. \( B_3B_2B_1B_0 \) as 1111 and \( A_3A_2A_1A_0 \) as 1101 for \( M \) as 1 is shown in Figure 5.

![Figure 5. Timing Diagram for a.](image)

The output Sum \( S_3S_2S_1S_0 \) is 1110 and the output carry \( C_4C_3C_2C_1 \) is 0001.

b. \( B_3B_2B_1B_0 \) as 1111 and \( A_3A_2A_1A_0 \) as 0101 for \( M \) as 0 is shown in Figure 6.

![Figure 6. Timing Diagram for b.](image)

The output Sum \( S_3S_2S_1S_0 \) is 0100 and the output carry is 1111. This verifies the working of the circuit.

The simulation of the schematic is done in the DSCH tool. The VERILOG File is generated and then this file is compiled in the Microwind Tool to obtain its physical layout. The simulation of the circuit is performed using the BSIM4 model. The Berkeley Short-Channel IGFET Model (BSIM) is a very elaborate model that is now widely used in circuit simulation.[7]

IV. Results and Discussions
Decrease in power consumption in digital circuits is of major concern as it improves the battery life. Power consumption issues can lead to over consumption of resources when devices are cascaded [8]. This power reduction will produce an overall increased delay.

This section presents the layout and analog simulations of the discussed circuit under different foundries such as 65nm and 45nm adder-subtractor. The analog simulation is performed using Microwind Lite 3.1 tool.

The circuit is simulated and compared for performance using this tool. Figure 7. Shows the layout of 65nm CMOS 4 bit adder-subtractor

The analog simulation of the circuit in 65nm Foundry is shown in Figure 8. The simulations are used to analyze and compare the performance of the circuits.

The analog simulation of the circuit in 65 nm CMOS Technology is shown in Figure 8. The simulations are used to analyze and compare the performance of the circuits.
Figure 9 shows the layout of 45nm CMOS 4 bit adder-subtractor. The layout shows the various metals layers and the polysilicon gate and their interconnections through via. The pMOS or the pull up network is shown at the top and the nMOS or the pull down network is shown at the bottom in the layout.

Analog simulation of 4 bit adder subtractor in 45nm foundry is shown in figure 10. The schematic of the circuit is designed and tested in DSCH 3.1 and then its VERILOG file is generated which is further compiled to obtain the analog simulation in the Microwind 3.1 Tool.

The analysis of the area and power consumption by the circuit is also performed by the Microwind designing Tool. The performance comparison between area and power of CMOS 4 bit adder-subtractor based on 65nm and 45nm, foundries is performed. The circuit is designed using 65nm and 45nm channel lengths and have layout width and height of 48.9µm/16.1µm and 35.0µm/11.5µm respectively.

### TABLE 2. Comparative Study of Power and Area

<table>
<thead>
<tr>
<th>Parameter</th>
<th>65nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area(µm²)</td>
<td>787.8</td>
<td>401.9</td>
</tr>
<tr>
<td>Power(µW)</td>
<td>50.222</td>
<td>2.937</td>
</tr>
</tbody>
</table>
The comparison of area and power consumption in 4 Bit Adder-Subtractor design based on different channel lengths is summarized in Table 2. The graphical analysis makes it clear that the area consumed by the 4 bit Adder-Subtractor circuit is minimum for the 45nm CMOS Technology. Area consumption by 65 nm CMOS Technology is reduced by 51% as compared to 90 nm CMOS Technology. The analysis also shows that the power consumed by the 45nm CMOS Technology is minimum. Power consumption of 65nm foundry is reduced by 94% as compared to 90nm CMOS Technology.

V. CONCLUSION
This paper studies the effect of various channel lengths on the power and area consumption of a 4 bit adder-subtractor circuit with overflow detection. The composite 4 bit Adder-Subtractor circuit is used instead of separate adder subtract circuit which saves resources. The power consumed by the composite circuit in 65nm and 45nm foundries is 50.22 µW and 2.937 µW respectively. The area consumed by the composite circuit in 65nm, 45nm, channel lengths is 787.8 µm² and 401.9 µm² respectively.

REFERENCES